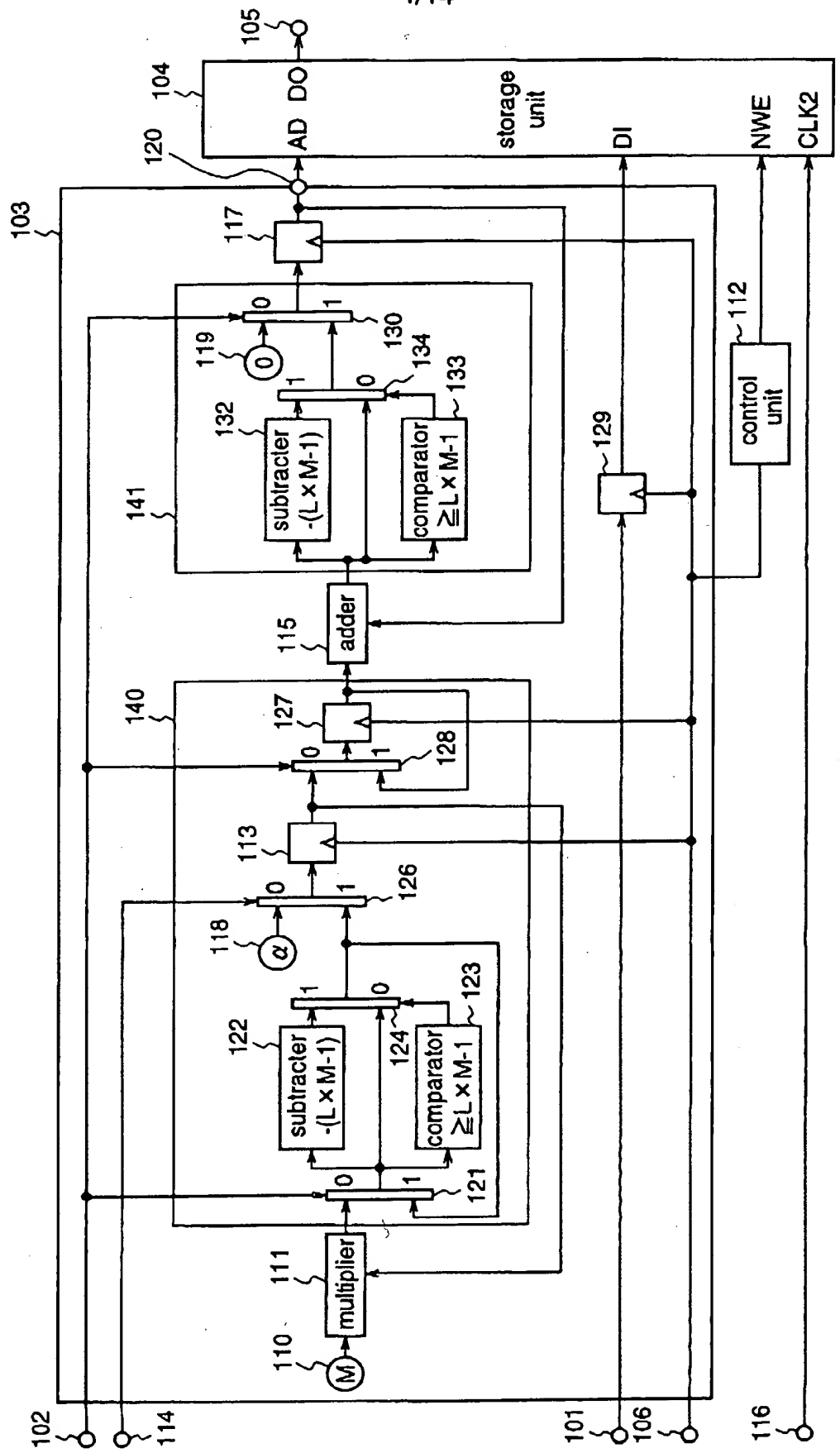

storage unit
AD
DO
DI
NWE
CLK2
control unit
multiplier
adder
subtracter -(L×M-1)
comparator ≧L×M-1
subtracter -(L×M-1)
comparator ≧L×M-1
M
α
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16

Fig.1

T0S00T* 0T99E660

Fig.2(a)

2

0	10	1	11	2
12	3	13	4	14
5	15	6	16	7
17	8	18	9	19

Fig.2(b)

10

0	2	4	6	8
10	12	14	16	18
1	3	5	7	9
11	13	15	17	19

Fig.2(c)

50-(19×2)=12

0	8	16	5	13
2	10	18	7	15
4	12	1	9	17
6	14	3	11	19

Fig.2(d)

60-(19×3)=3

0	13	7	1	14
8	2	15	9	3
16	10	4	17	11
5	18	12	6	19

Fig.2(e)

15

0	14	9	4	18
13	8	3	17	12
7	2	16	11	6
1	15	10	5	19

Fig.2(f)

75-(19×3)=18

0	18	17	16	15
14	13	12	11	10
9	8	7	6	5
4	3	2	1	19

Fig.2(g)

90-(19×4)=14

0	15	11	7	3
18	14	10	6	2
17	13	9	5	1
16	12	8	4	19

Fig.2(h)

70-(19×3)=13

0	3	6	9	12
15	18	2	5	8
11	14	17	1	4
7	10	13	16	19

Fig.2(i)

65-(19×3)=8

0	12	5	17	10
3	15	8	1	13
6	18	11	4	16
9	2	14	7	19

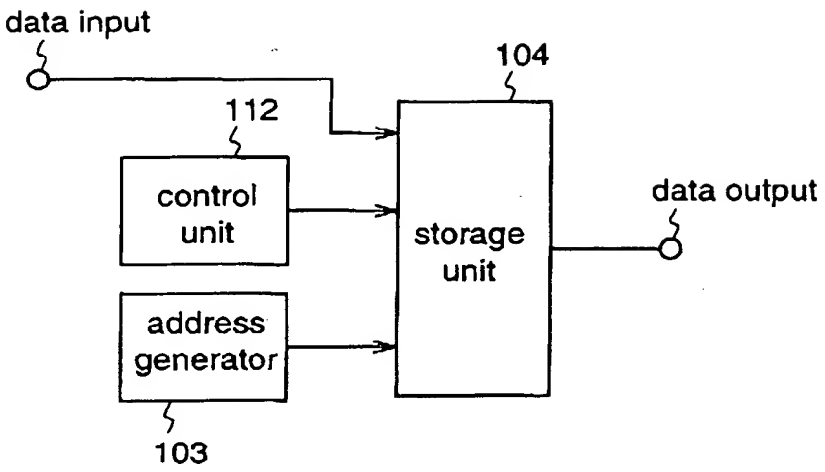
Fig.2(j)

40-(19×2)=2

0	10	1	11	2
12	3	13	4	14
5	15	6	16	7
17	8	18	9	19

09/936510

Fig.3


data input
104
112
control unit
storage unit
data output
address generator
103

09/936510

Fig.4

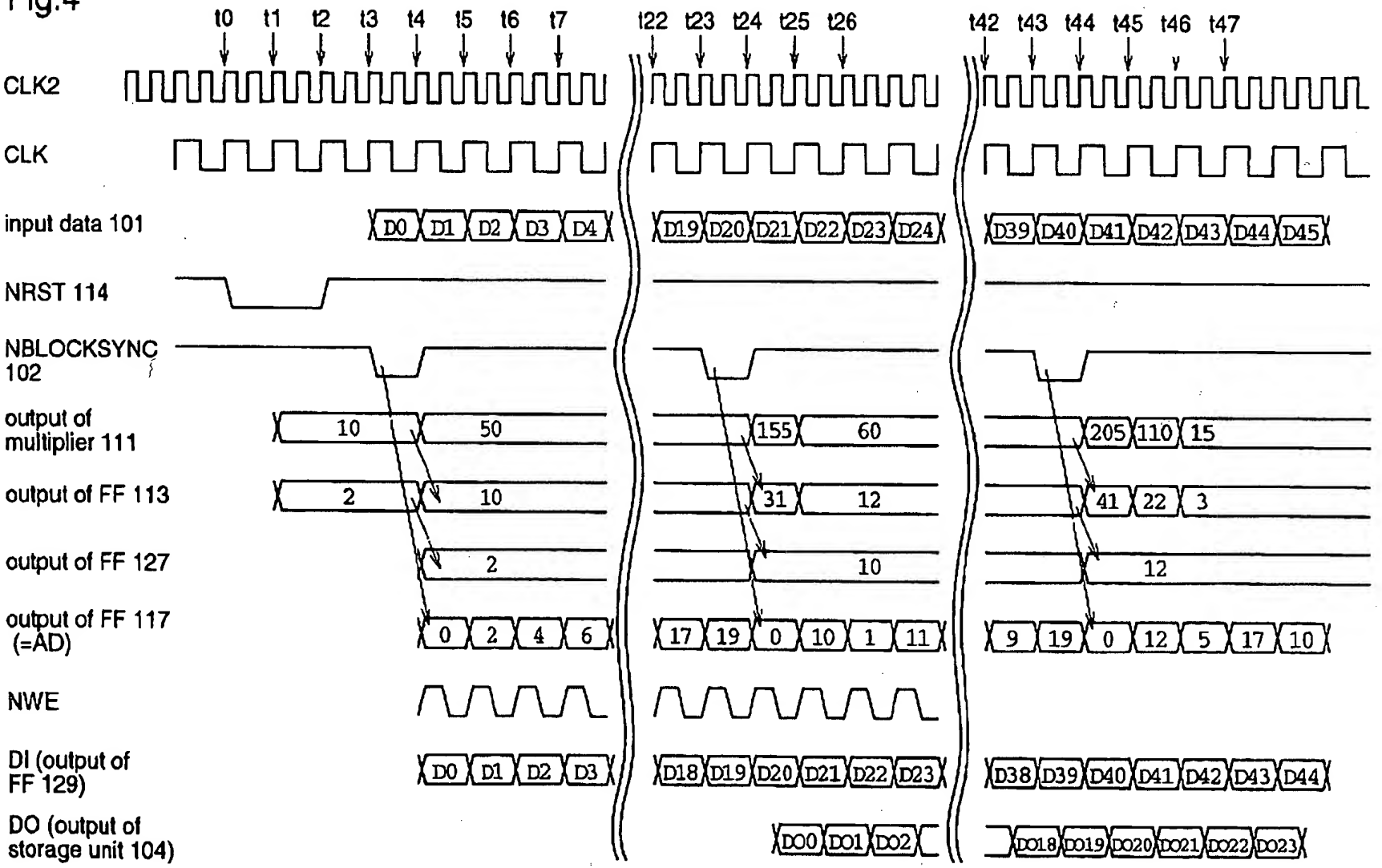


Fig.5

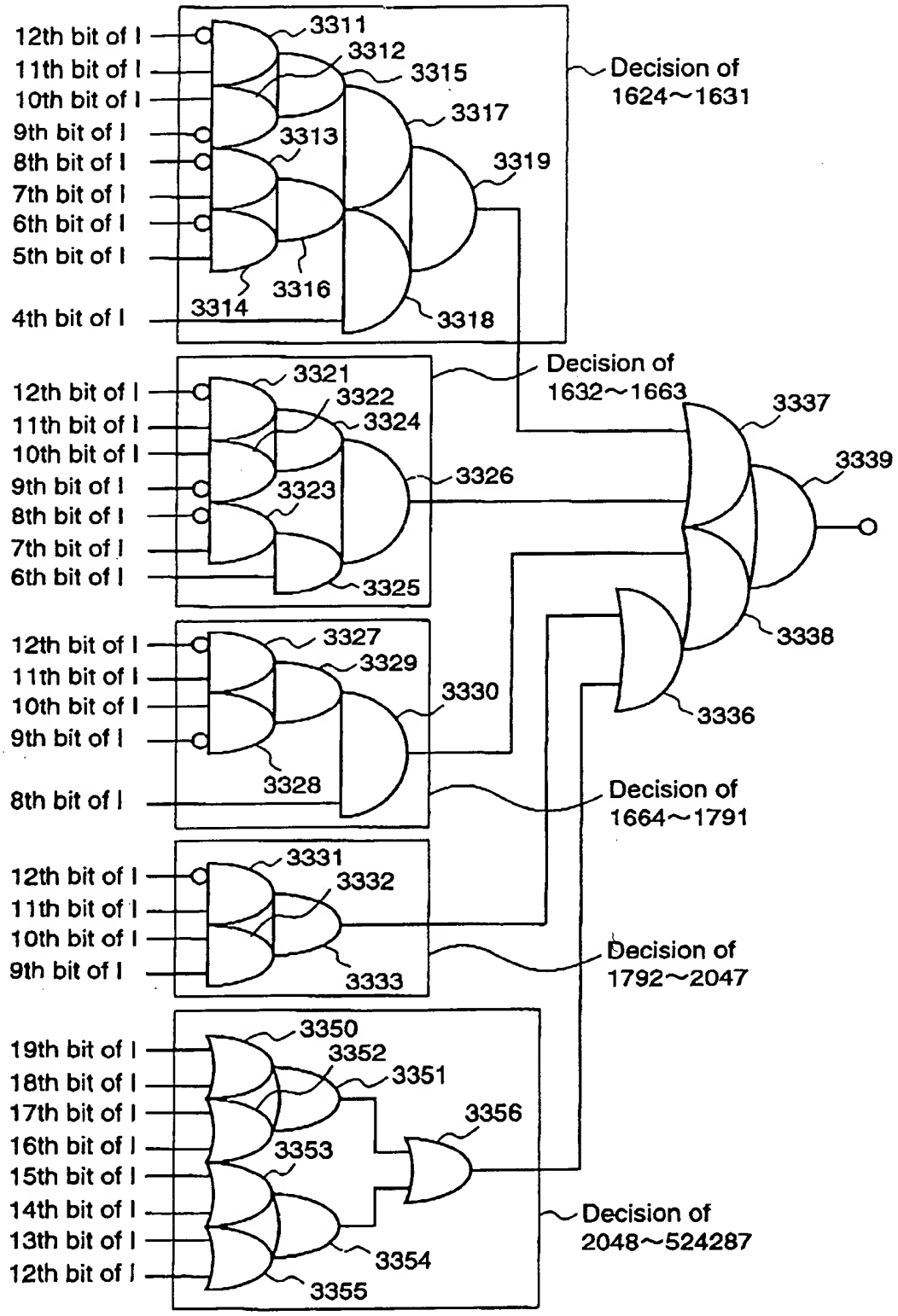
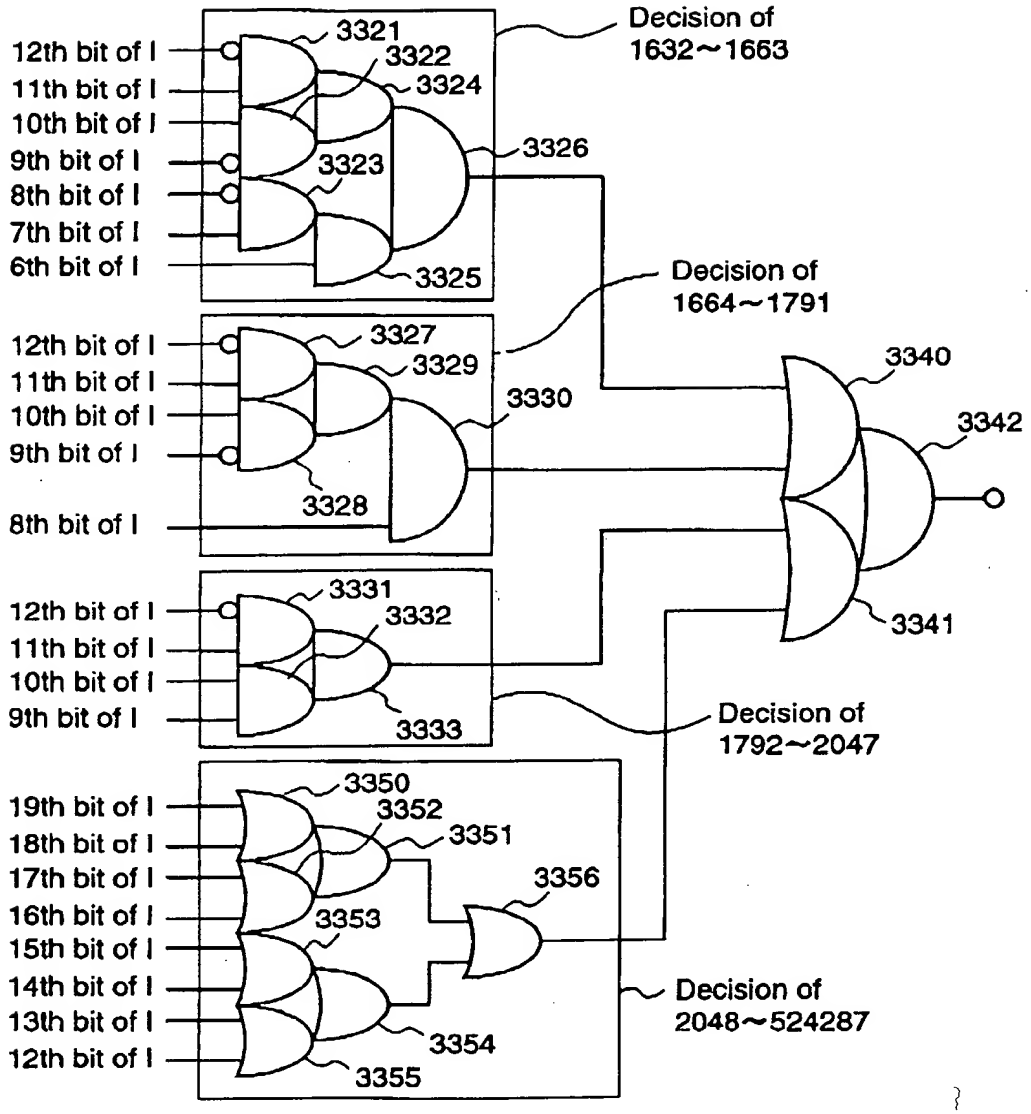

12th bit of I
11th bit of I
10th bit of I
9th bit of I
8th bit of I
7th bit of I
6th bit of I
5th bit of I
4th bit of I
3311
3312
3315
3317
3313
3319
3316
3314
3318
Decision of 1624~1631
3321
3322
3324
3326
3323
3325
Decision of 1632~1663
3337
3339
3338
3336
3327
3329
3330
3328
Decision of 1664~1791
3331
3332
3333
Decision of 1792~2047
19th bit of I
18th bit of I
17th bit of I
16th bit of I
15th bit of I
14th bit of I
13th bit of I
12th bit of I
3350
3352
3351
3356
3353
3354
3355
Decision of 2048~524287

Fig.6


12th bit of I
11th bit of I
10th bit of I
9th bit of I
8th bit of I
7th bit of I
6th bit of I
3321
3322
3323
3324
3325
3326
Decision of
1632~1663
12th bit of I
11th bit of I
10th bit of I
9th bit of I
8th bit of I
3327
3328
3329
3330
Decision of
1664~1791
12th bit of I
11th bit of I
10th bit of I
9th bit of I
3331
3332
3333
Decision of
1792~2047
19th bit of I
18th bit of I
17th bit of I
16th bit of I
15th bit of I
14th bit of I
13th bit of I
12th bit of I
3350
3351
3352
3353
3354
3355
3356
Decision of
2048~524287
3340
3341
3342

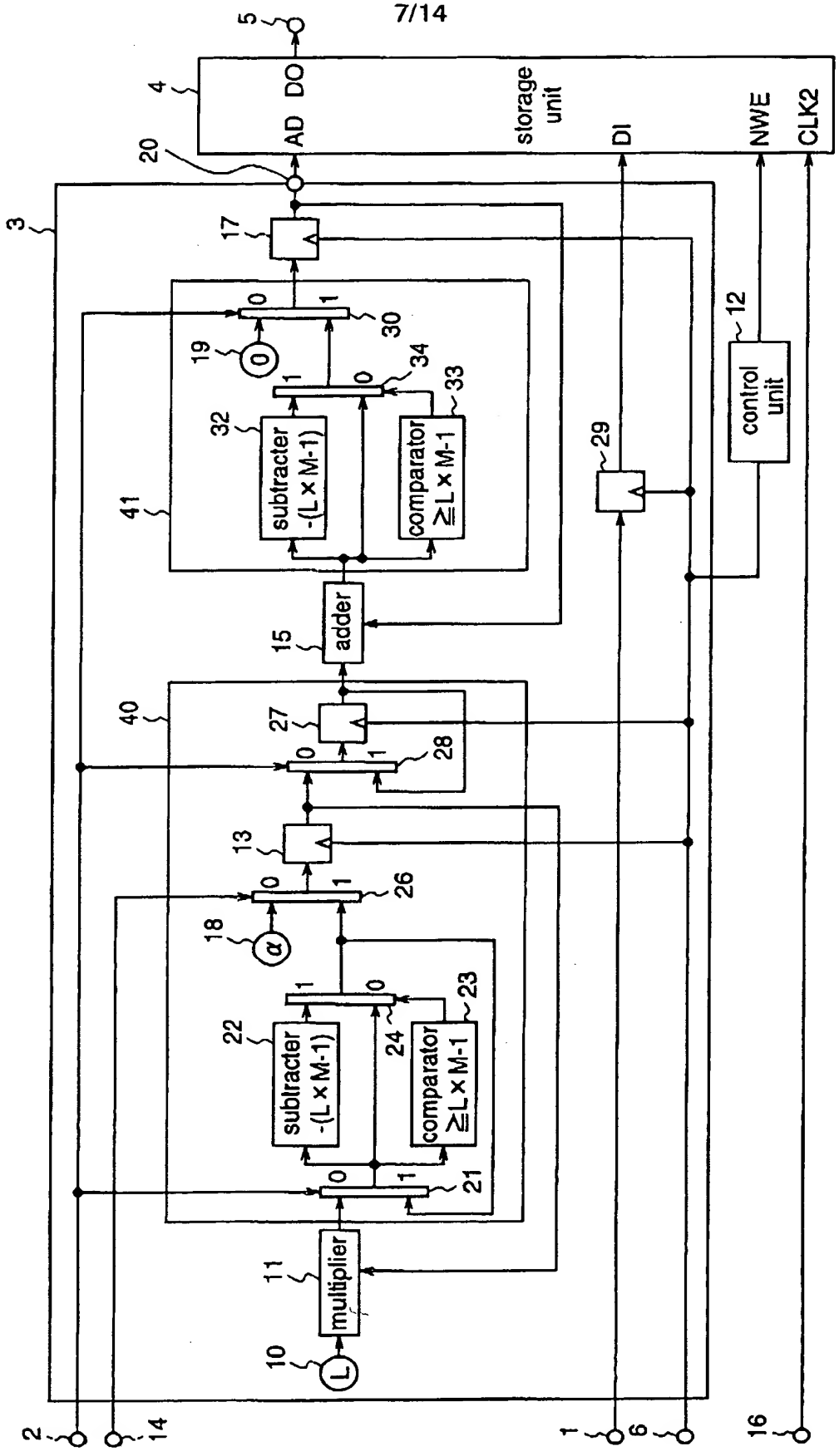

5
4
AD
DO
storage unit
DI
NWE
CLK2
20
3
17
0
1
30
19
0
34
1
0
32
subtracter -(L×M-1)
comparator ≧L×M-1
33
41
29
12
control unit
15
adder
40
27
28
13
26
18
α
22
24
23
21
11
multiplier
10
L
2
14
1
6
16

Fig.7

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Fig.8(a)

2

0	10	1	11	2
12	3	13	4	14
5	15	6	16	7
17	8	18	9	19

Fig.8(b)

8

0	12	5	17	10
3	15	8	1	13
6	18	11	4	16
9	2	14	7	19

Fig.8(c)

32-19=13

0	3	6	9	12
15	18	2	5	8
11	14	17	1	4
7	10	13	16	19

Fig.8(d)

52-(19×2)=14

0	15	11	7	3
18	14	10	6	2
17	13	9	5	1
16	12	8	4	19

Fig.8(e)

56-(19×2)=18

0	18	17	16	15
14	13	12	11	10
9	8	7	6	5
4	3	2	1	19

Fig.8(f)

72-(19×3)=15

0	14	9	4	18
13	8	3	17	12
7	2	16	11	6
1	15	10	5	19

Fig.8(g)

60-(19×3)=3

0	13	7	1	14
8	2	15	9	3
16	10	4	17	11
5	18	12	6	19

Fig.8(h)

12

0	8	16	5	13
2	10	18	7	15
4	12	1	9	17
6	14	3	11	19

Fig.8(i)

48-(19×2)=10

0	2	4	6	8
10	12	14	16	18
1	3	5	7	9
11	13	15	17	19

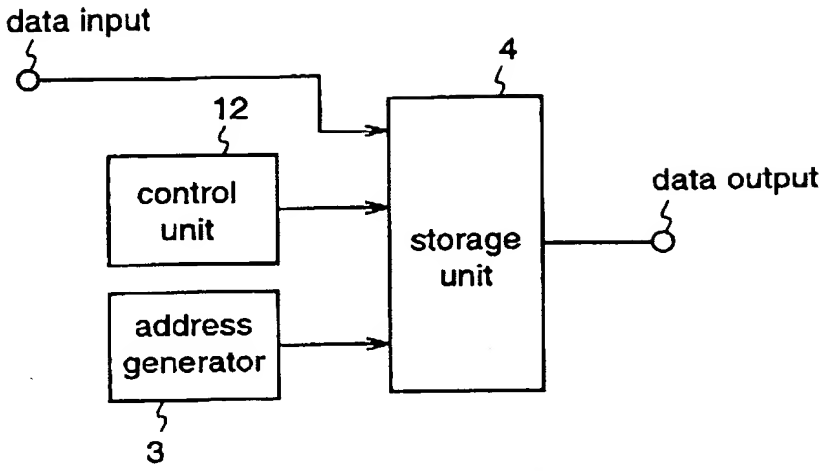
Fig.8(j)

40-(19×2)=2

0	10	1	11	2
12	3	13	4	14
5	15	6	16	7
17	8	18	9	19

09/936510

Fig.9


data input
4
12
control unit
storage unit
data output
address generator
3

09/936510

Fig.10

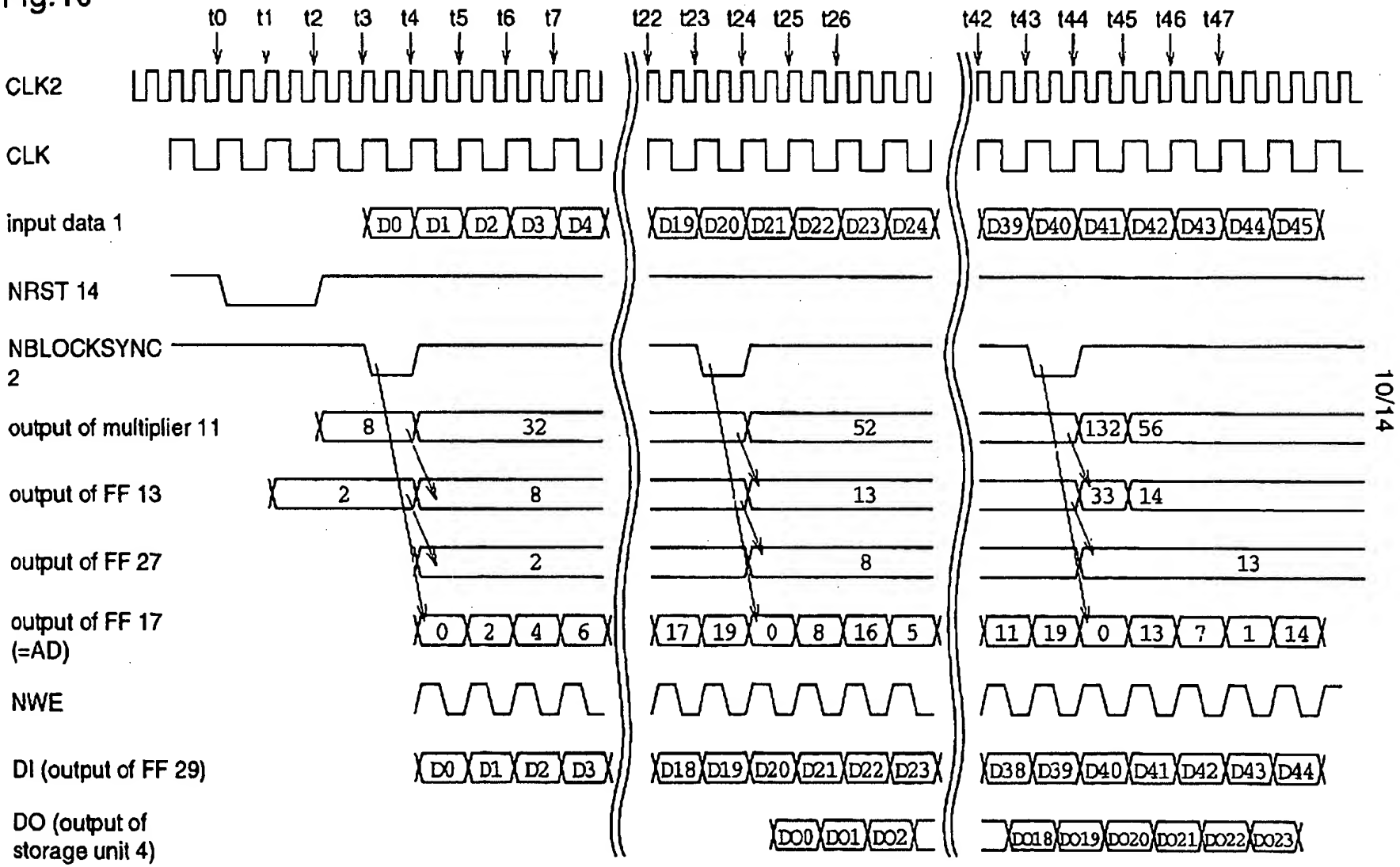


Fig.11

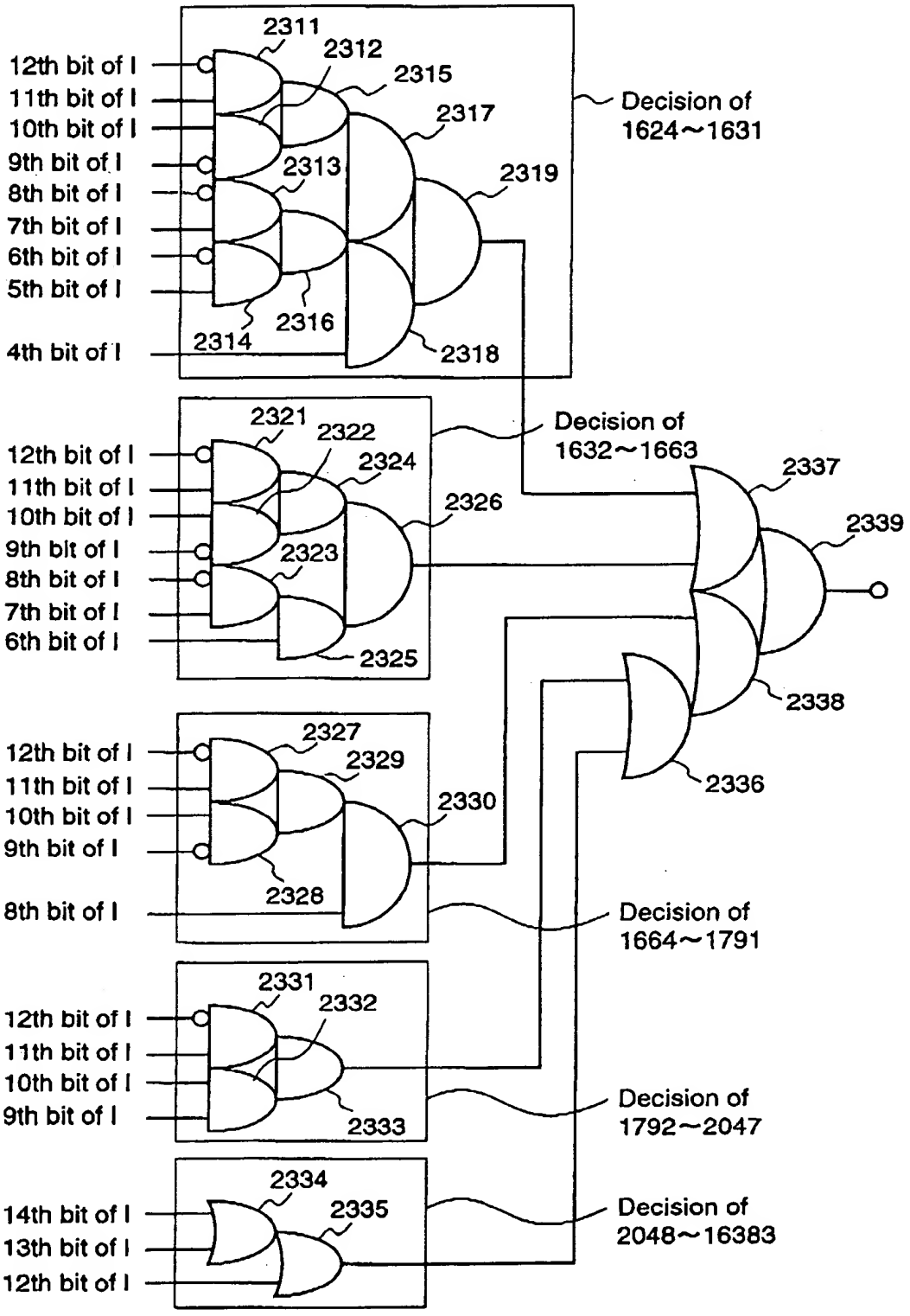

2311
2312
2315
2317
2319
12th bit of I
11th bit of I
10th bit of I
9th bit of I
8th bit of I
7th bit of I
6th bit of I
5th bit of I
4th bit of I
2313
2314
2316
2318
Decision of
1624~1631
2321
2322
2324
2326
2323
2325
Decision of
1632~1663
2337
2339
2338
2336
2327
2329
2330
2328
Decision of
1664~1791
2331
2332
2333
Decision of
1792~2047
2334
2335
14th bit of I
13th bit of I
12th bit of I
Decision of
2048~16383

Fig.12

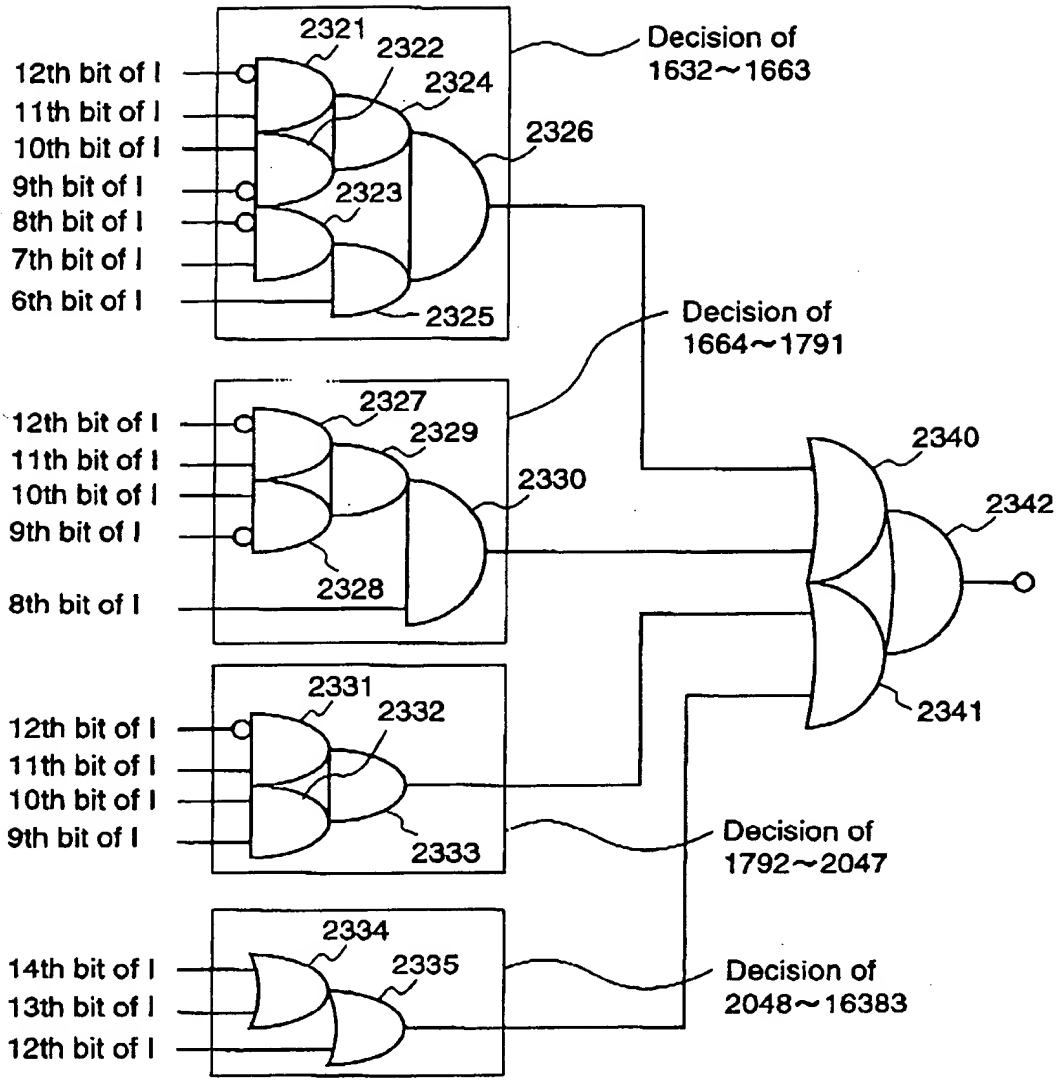

2321
2322
2324
2326
2323
2325
12th bit of I
11th bit of I
10th bit of I
9th bit of I
8th bit of I
7th bit of I
6th bit of I
Decision of
1632~1663
2327
2329
2330
2328
12th bit of I
11th bit of I
10th bit of I
9th bit of I
8th bit of I
Decision of
1664~1791
2340
2342
2341
2331
2332
2333
12th bit of I
11th bit of I
10th bit of I
9th bit of I
Decision of
1792~2047
2334
2335
14th bit of I
13th bit of I
12th bit of I
Decision of
2048~16383

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Fig.13(a)

1

0	1	2	3	4
5	6	7	8	9
10	11	12	13	14
15	16	17	18	19

Fig.13(b)

5

0	4	8	12	16
1	5	9	13	17
2	6	10	14	18
3	7	11	15	19

Fig.13(c)

25-19=6

0	16	13	10	7
4	1	17	14	11
8	5	2	18	15
12	9	6	3	19

Fig.13(d)

30-19=11

0	7	14	2	9
16	4	11	18	6
13	1	8	15	3
10	17	5	12	19

Fig.13(e)

55-(19×2)=17

0	9	18	8	17
7	16	6	15	5
14	4	13	3	12
2	11	1	10	19

Fig.13(f)

85-(19×4)=9

0	17	15	13	11
9	7	5	3	1
18	16	14	12	10
8	6	4	2	19

Fig.13(g)

45-(19×2)=7

0	11	3	14	6
17	9	1	12	4
15	7	18	10	2
13	5	16	8	19

Fig.13(h)

35-19=16

0	6	12	18	5
11	17	4	10	16
3	9	15	2	8
14	1	7	13	19

Fig.13(i)

80-(19×4)=4

0	5	10	15	1
6	11	16	2	7
12	17	3	8	13
18	4	9	14	19

Fig.13(j)

20-19=1

0	1	2	3	4
5	6	7	8	9
10	11	12	13	14
15	16	17	18	19

Fig.13(k)

1

0	1	2	3	4
5	6	7	8	9
10	11	12	13	14
15	16	17	18	19

Fig.13(l)

4

0	5	10	15	1
6	11	16	2	7
12	17	3	8	13
18	4	9	14	19

Fig.13(m)

16

0	6	12	18	5
11	17	4	10	16
3	9	15	2	8
14	1	7	13	19

Fig.13(n)

64-(19×3)=7

0	11	3	14	6
17	9	1	12	4
15	7	18	10	2
13	5	16	8	19

Fig.13(o)

28-19=9

0	17	15	13	11
9	7	5	3	1
18	16	14	12	10
8	6	4	2	19

Fig.13(p)

36-19=17

0	9	18	8	17
7	16	6	15	5
14	4	13	3	12
2	11	1	10	19

Fig.13(q)

68-(19×3)=11

0	7	14	2	9
16	4	11	18	6
13	1	8	15	3
10	17	5	12	19

Fig.13(r)

44-(19×2)=6

0	16	13	10	7
4	1	17	14	11
8	5	2	18	15
12	9	6	3	19

Fig.13(s)

24-19=5

0	4	8	12	16
1	5	9	13	17
2	6	10	14	18
3	7	11	15	19

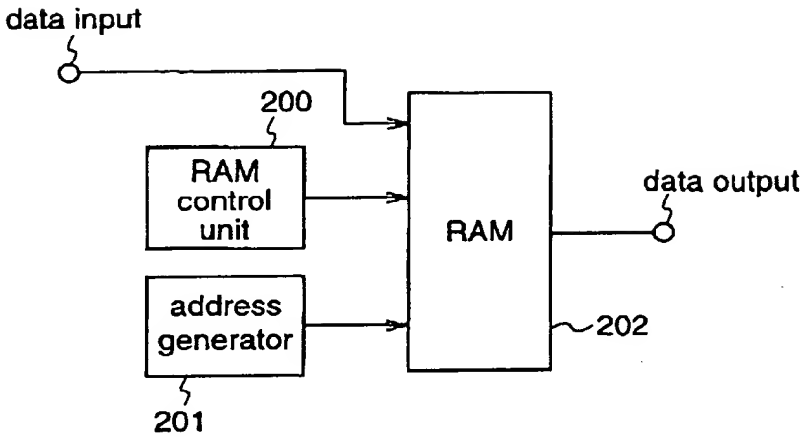
Fig.13(t)

20-19=1

0	1	2	3	4
5	6	7	8	9
10	11	12	13	14
15	16	17	18	19

09/936510

Fig.14


data input
200
RAM control unit
address generator
201
RAM
data output
202